

AMENDMENT(S) TO THE CLAIMS

1 **1.** (canceled)

2 **2.** (canceled)

3 **3.** (canceled)

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1 **12. (canceled)**

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1 **24. (canceled)**

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6 **29. (canceled)**

7 **30. (canceled)**

8 **31. (canceled)**

9 **32. (canceled)**

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1 33. (previously presented): An integrated circuit, comprising:
2 a plurality of data receivers that evaluate corresponding data signals relative
3 to a distributed reference voltage;
4 a feedback receiver that evaluates the distributed reference voltage relative
5 to a nominal reference voltage to produce a feedback signal;
6 a reference voltage driver that produces a compensated reference voltage;
7 wherein the compensated reference voltage is routed on the integrated
8 circuit to form the distributed reference voltage at the data and feedback receivers,
9 and the input characteristics of the data and feedback receivers cause a voltage
10 change in the distributed reference voltage at each receiver relative to the
11 compensated reference voltage;
12 wherein the data and feedback receivers have similar input characteristics
13 so that said relative voltage change in the distributed reference voltage is
14 approximately the same at each of the data and feedback receivers;
15 wherein the reference voltage driver includes an increment/decrement
16 component that produces a digital value in response to the feedback signal,
17 wherein the increment/decrement component is configured to increment and
18 decrement the digital value depending on the relationship of the distributed
19 reference voltage and the nominal reference voltage as indicated by the feedback
20 signal; and
21 wherein the reference voltage driver has a variable gain that is established
22 by the digital value.

1 34. (original): An integrated circuit as recited in claim 33, wherein the
2 compensated reference voltage is distributed over impedance-matched conductors
3 to form the distributed reference voltage at the data and feedback receivers.

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5 35. (original): An integrated circuit as recited in claim 33, wherein the
6 increment/decrement component is enabled during an initialization period and the
7 digital value remains constant during a subsequent operational period.

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9 36. (original): An integrated circuit as recited in claim 33, further
10 comprising a register that is configurable to store the digital value and to provide
11 the digital value to the reference voltage driver.

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13 37. (previously presented): An integrated circuit as recited in claim 33,
14 further comprising a register that is configurable to store the digital value and to
15 provide the digital value to the reference voltage driver, wherein the register is
16 readable and writable.

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18 38. (original): An integrated circuit as recited in claim 33, further
19 comprising a digitally controllable variable resistor that controls the gain of the
20 reference voltage driver.

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22 39. (original): An integrated circuit as recited in claim 33, wherein the
23 feedback receiver comprises a low-pass filter that does not significantly affect the
24 input characteristics of the feedback receiver.

1 **40.** (original): An integrated circuit as recited in claim 33, wherein the
2 distributed reference voltage is routed similarly to the data and feedback receivers
3 so that said relative voltage change in the distributed reference voltage is
4 approximately the same at each of the data and feedback receivers.

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6 **41.** (original): An integrated circuit as recited in claim 33, wherein:
7 the distributed reference voltage is routed similarly to the data and feedback
8 receivers so that said relative voltage change in the distributed reference voltage is
9 approximately the same at each of the data and feedback receivers; and
10 the feedback receiver comprises a low-pass filter that does not significantly
11 affect the input characteristics of the feedback receiver.

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13 **42.** (original): An integrated circuit as recited in claim 33, wherein the
14 integrated circuit is a memory device that further comprises a plurality of memory
15 storage cells.

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17 **43.** (canceled)

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19 **44.** (canceled)

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21 **45.** (canceled)

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23 **46.** (canceled)

1 47. (previously presented): An integrated circuit, comprising:
2 receiver means for evaluating a plurality of data signals relative to a
3 distributed reference voltage;
4 feedback means for evaluating the distributed reference voltage relative to a
5 nominal reference voltage to produce a feedback signal;
6 driver means having a variable gain for producing a compensated reference
7 voltage;
8 routing means for routing the compensated reference voltage on the
9 integrated circuit to form the distributed reference voltage at the receiver and
10 feedback means;
11 wherein the input characteristics of the receiver and feedback means cause
12 a voltage change in the distributed reference voltage at the receiver and feedback
13 means relative to the compensated reference voltage;
14 wherein the receiver and feedback means have similar input characteristics
15 so that said relative voltage change in the distributed reference voltage is
16 approximately the same at each of the receiver and feedback means; and
17 gain control means for controlling the gain of the driver means in response
18 to the feedback signal so that the distributed reference voltage is approximately
19 equal to the nominal reference voltage;
20 wherein the compensated reference voltage is distributed over impedance-
21 matched conductors to form the distributed reference voltage at the receiver and
22 feedback means.

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24 48. (canceled)
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1 **49. (canceled)**

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1 54. (previously presented): A memory device comprising:
2 a plurality of memory storage cells that are capable of storing data;
3 a plurality of data receivers that evaluate binary data signals with reference
4 to a distributed reference voltage and that are coupled to the plurality of memory
5 storage cells;
6 a feedback receiver that evaluates the distributed reference voltage relative
7 to a nominal reference voltage to produce a feedback signal;
8 a reference voltage driver that produces a compensated reference voltage;
9 wherein the compensated reference voltage is routed on the memory device
10 to form the distributed reference voltage at the data and feedback receivers, and
11 the input characteristics of the data and feedback receivers cause a voltage change
12 in the distributed reference voltage at each receiver relative to the compensated
13 reference voltage;
14 wherein the data and feedback receivers have similar input characteristics
15 so that said relative voltage change in the distributed reference voltage is
16 approximately the same at each of the data and feedback receivers; and
17 wherein the reference voltage driver has a variable gain that is configurable
18 to increase in response to the feedback signal when the distributed reference
19 voltage is less than the nominal reference voltage and to decrease in response to
20 the feedback signal when the distributed reference voltage is greater than the
21 nominal reference voltage;
22 wherein the compensated reference voltage is distributed over impedance-
23 matched conductors to form the distributed reference voltage at the data and
24 feedback receivers.

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1 55. (canceled)

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